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DESIGN OF LOW POWER AND AREA EFFICIENT HYBRID LINEAR FEEDBACK SHIFT REGISTER

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ABSTRACT: Gate Diffusion Input (GDI) technique reduces the power, delay and also maintains a less complex logic design. But GDI based Linear Feedback Shift Register (LFSR) needs a larger number of transistors for the construction of D flip-flop due to which the area required will be more than the conventional model. So, we have to reduce the transistor count to reduce power dissipation. This paper proposed hybrid 4-bit LFSR which is the combination of both conventional and GDI models. The proposed hybrid 4-bit LFSR can be designed using both conventional D flip-flop and GDI based XOR gate using Cadence Virtuoso with 90nm technology library. The performances of area, power and delay parameters were obtained using Cadence Spectra simulator, Digital Schematic and Micro Wind tools. The proposed hybrid 4-bit LFSR model achieved better performances of delay and power parameters as compared with other existing models. From the simulation results, it is clearly observed that 62.12% power reduced compared to conventional LFSR, 26.71% power reduced compared to GDI, 59.40% delay reduced compared to conventional and 66.75 % delay reduced compared to GDI.

KEYWORDS: Gate Diffusion Input, Linear Feedback Shift Register, Cadence, Digital Schematic, Micro Wind.

I. INTRODUCTION

With the continuous development and progress in technology which was scaling billion ranges of transistors which can be incorporated on a single chip that has brought fantastic adjustments in its functionality. However together with that it has also expanded the time for the checking out method. Power dissipation is a simple parameter in system of testing because the circuit disperses greater strength at some point of the preliminary than its typical running. Elevated electricity dissipation also leads to growth inside the chips and consumes more contemporary at once from the power deliver. Electricity dissipation at some stage in the checking out should be as low as possible within the VLSI era [4-6]. Compared to the inner trying out automatic check equipment (ATE) is the disadvantage of outside trying out which turned into as a substitute very high priced, takes extra time for checking out and inefficient. BIST gives proper solutions to these issues because it works on self trying out mechanism that is aggregate “built-in check” and “self-check”. LFSR generates pseudo-random sequences that are used within the BIST. On-chip test generation makes use of this pseudo random testing advantage which is designed with simple hardware [1].

II. RELATED WORK

The described technique i.e., Gate Diffusion Input is a low power digital circuit design. Maintaining the low complexity of the logic design, this technique shows less delay and consumes less area with less power.

2.1 Conventional LFSR

LFSR is a type of shift register which works on the linear function of the previous input. As XOR is the only linear function of single bits, this register is functioned based on the input value from the XOR of some bits of overall register value. The preliminary value taken by the shift register is called seed value and due to the deterministic operation the register, the continuous stream of values generated by the register completely

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depends on its previous value. Due to the finite possible states of the shift register, there will be eventually entering of a repeating cycle. Digital signal processing (DSP) and communication systems are the two major streams which uses these LFSR structures such as Binary Coded Hexadecimal (BCH), Cyclic redundancy check (CRC). Linear Feedback Shift Register is serial arrangement of the d flip flops where the present flip flop's output depends on the previous flip flop's input. The seed value of the shift register is the combination of series of 1's and 0's. The seed value is the most important as the power dissipation depends on it as it determines further random values. As there are finite numbers of possibilities LFSR enters a repeating cycle [2-3].

LFSR is of two types

i. External /Standard LFSR

ii. Internal /Modular LFSR

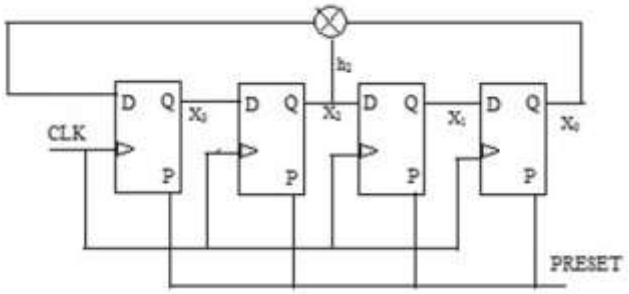

Fig. 1: 4-Bit External LFSR

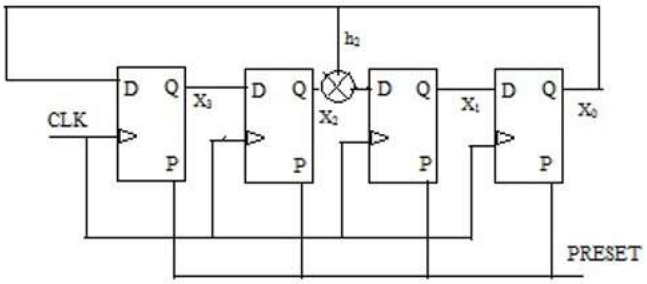

Fig. 2: 4-Bit Internal LFSR

The above shown Figure 1 and Figure 2 represents the both types of LFSRs. As compared to the standard LFSR delay of the modular LFSR is decreased. In the modular LFSR due to the absence of the various XOR gate outputs the delay is less and the last and first flips are directly connected.

2.1.1. Conventional D Flip-Flop

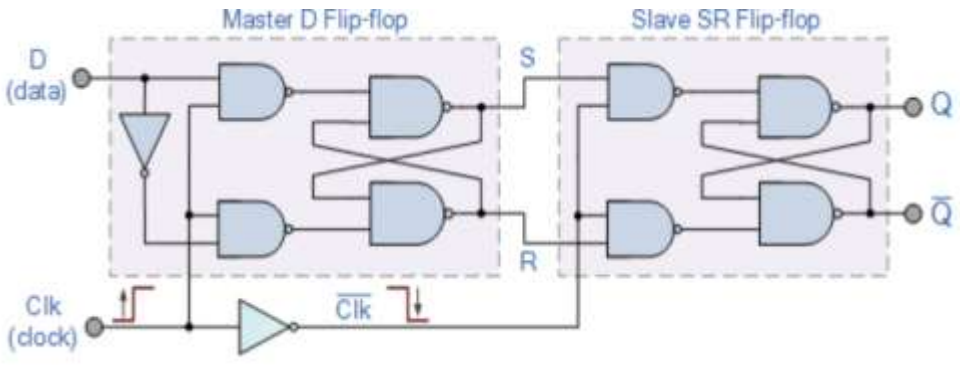

Fig. 3: Conventional D Flip-Flop

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There will be no output in the circuit when the clock input is not applied to the D flip flop or during the falling edge of the clock signal. The practicality of the D flip flop may be increased by combining with SR flip flop to its output that is activated on the complementary clock signal that offers rise to production of a "Master-Slave D-type flip flop". A D-type flip flop may be improved additional by adding a second SR flip-flop to its output that's activated on the complementary clock signal to provide a "Master-Slave D-type flip flop". throughout the rising fringe of the clock signal the primary stage, the "master" latches the input condition at D, whereas the output stage is deactivated and through the falling fringe of the clock signal the second "slave" stage is currently activated, latching on to the output driven from the primary master circuit. Then the output stage seems to be triggered on the negative fringe of the clock pulse. "Master-Slave D-type flip flops" may be designed by the cascading along of 2 latches with opposite clock phases.

2.1.2. Conventional XOR Gate

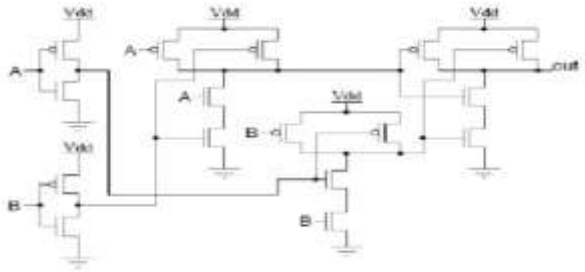

Fig. 4: Conventional 2-Input XOR Gate

The above shown design for the XOR gate improves both the power and speed. Figure 4 represents the basic design of the conventional XOR gate based on CMOS technology. Many Arithmetic circuits use these as the basic building blocks. This paper contrasts and evaluates the performance of conventional CMOS based XOR circuit design. It is based on the study of high speed, low power, and small area in XOR digital circuits. . The above shown figure 4 shows the preliminary design of the XOR gate using the CMOS .These XOR gates can be designed using CMOS technology have been using Cadence VIRTUOSO with the voltages 0.2 to 1.2 voltages at the temperature of 27℃. Figure 5 shows simulation results show the delay product, power, delay product (PDP), and average dynamic power consumption.

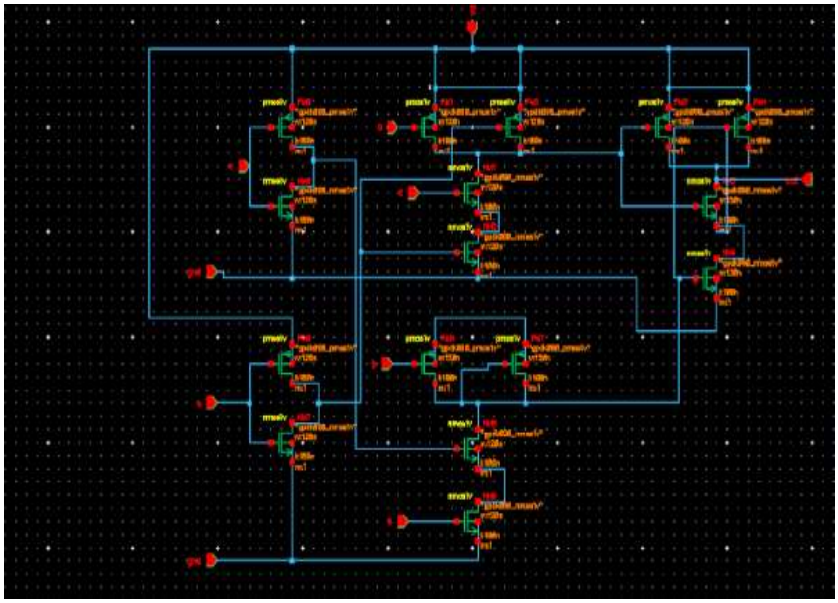

Fig. 5: Conventional XOR Gate Schematic using Cadence Virtuoso

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III. GDI Based Linear Feed Back Shift Register

3.1. Gate Diffusion Input Technique

The basic Gate-Diffusion Input cell is shown in figure 6. At first sight, you think, it is an inverter circuit, but with all similarity it is not. Because the source of the PMOS in a GDI cell is not connected to VDD, also the source of the NMOS in a GDI cell is not connected to ground. This GDI basic cell consists of two extra pins with some advantages and some disadvantages over the CMOS technology. The main disadvantage of this GDI technology is that it requires two twin-well CMOS or silicon on insulator (SoI) process to implement which is rather more expensive than the standard p-well CMOS process. Due to the more advancement in the CMOS technology so there are various types of efficient designing of the VLSI technology .Some of the types are PTL, CMOS and Gate Diffusion Input (GDI) techniques. GDI helps in designing the digital circuits where the energy required will be very less compared to the CMOS technology by which we can overcome some of the flaws of the PTL and CMOS techniques.

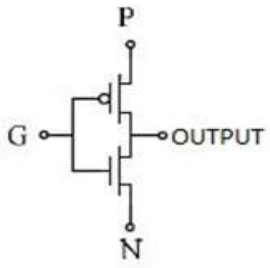

Fig. 6: Basic GDI Cell

Three input cells of GDI cell - G (common gateway for NMOS and PMOS), P (input / source for PMOS) and N (source input / disposal for NMOS). Both the NMOS and PMOS brakes are connected to the N and the Success. Table 1 shows the different cracking functions used with different values of GDI logic With the GDI scheme different logic functions can be implemented at high speed and low power compared to the standard CMOS architecture.

Table. 1: GDI Implemented Logic Functions

P	G	N	Function	Output
A	B	0	F_1	B'A
1	B	A	F_2	B'+A
A	B	1	OR	B+A
0	B	A	AND	BA
A	B	C	MUX	B'A+BC
1	B	0	NOT	B

The following characters can be reduced using this technique:

- Propagation delay
- Power consumption
- Low complexity logic designed Area digital circuits

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The below mentioned factors shows the advantages of GDI compared to the CMOS Technology

- Area layout
- Transistor count
- Delay
- Power dissipation

3.2. GDI based XOR Gate

By using the GDI technique, the number of transistors used will be less and the power dissipation will also be reduced. The designing of the XOR gate using the GDI technique can be observed in the figure 7.

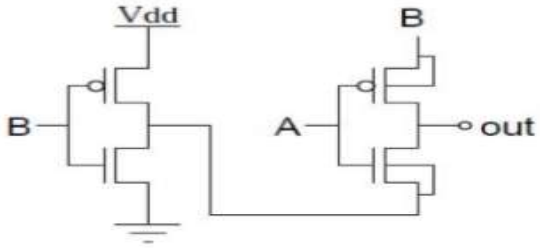

Fig. 7: GDI Based XOR Gate

It is two input XOR gate where A and B are two inputs output is 0 when there is two equal input; in remaining cases output is 1.

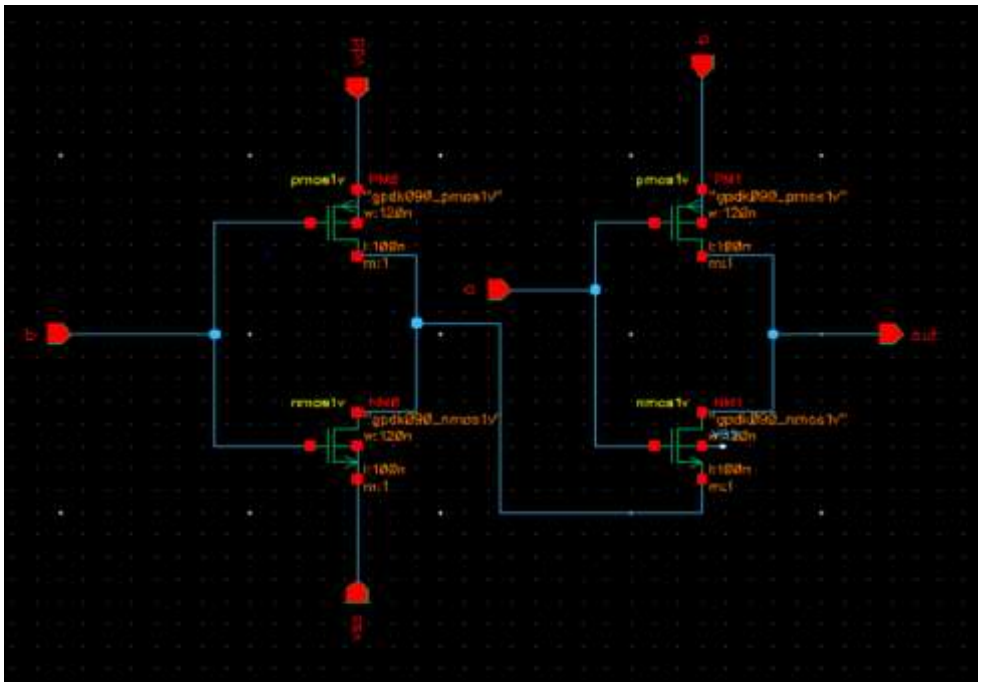

Fig. 8: GDI Based XOR Schematic using Cadence Virtuoso

3.3. GDI based D Flip Flop

The implementation of the D flip-flop can be observed in the figure 9 using the GDI technique. Mainly GDI was used to reduce the power delay product and to increase the performance of the circuit. The d flip-flop are mainly of two types i.e., single edge-triggered and double edge-triggered. But due to the sampling of the data on both the

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clock edges, the double edge-triggered lacks in the performance degradation. Single edge-triggered flip-flops are simply designed and samples clock on only one clock edge. By using the Master-slave configuration, these flip flops are designed. The components of the circuit are body gates and the inverter.

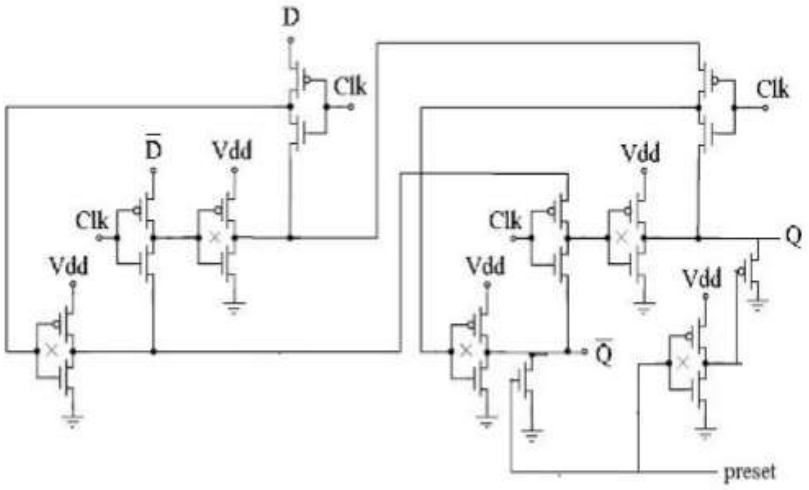

Fig. 9: GDI Based D Flip-Flop

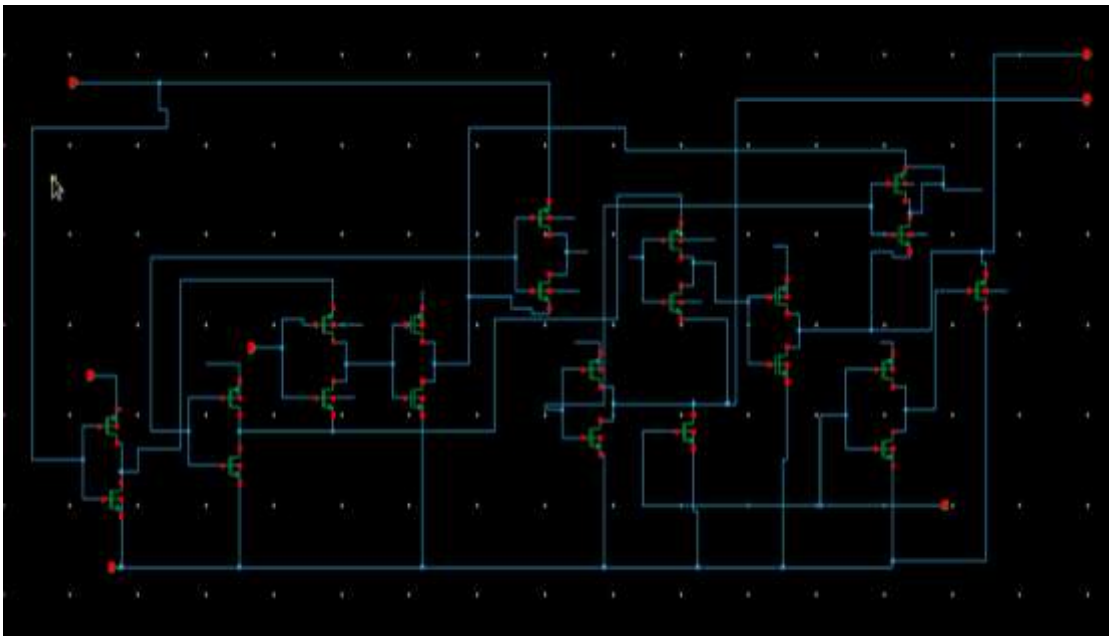

Fig. 10: GDI Based D Flip-Flop Schematic using Cadence Virtuoso

3.4. GDI Based LFSR

LFSR is designed using the GDI technique in the figure 11 which the combination of GDI based D flip-flop and GDI based XOR gate in the Cadence virtuoso software tool. This structure is designed for better area, speed and to reduce the power dissipation.

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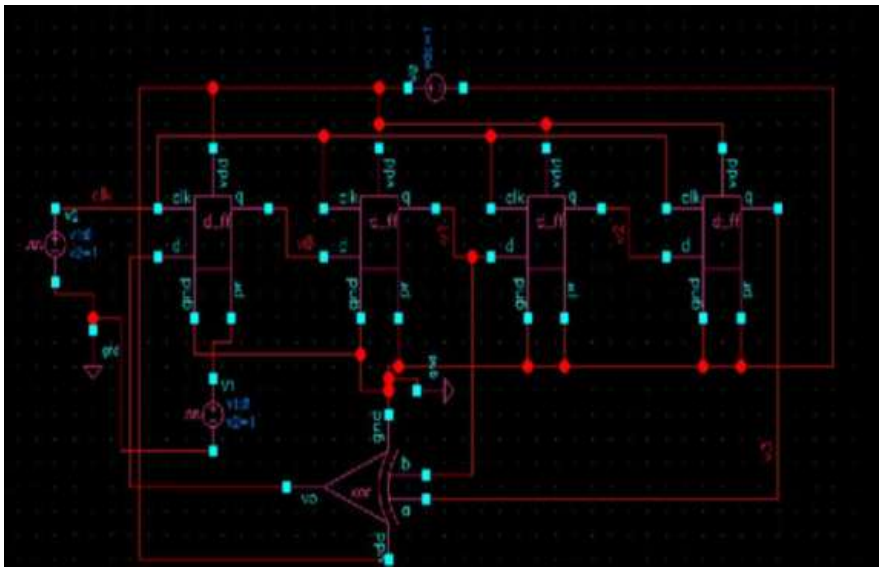

Fig. 11: GDI Based LFSR

3.5. GDI based LFSR

GDI based LFSR where D flip-flop and XOR are implemented using the GDI technique which can be observed in the figure 12.

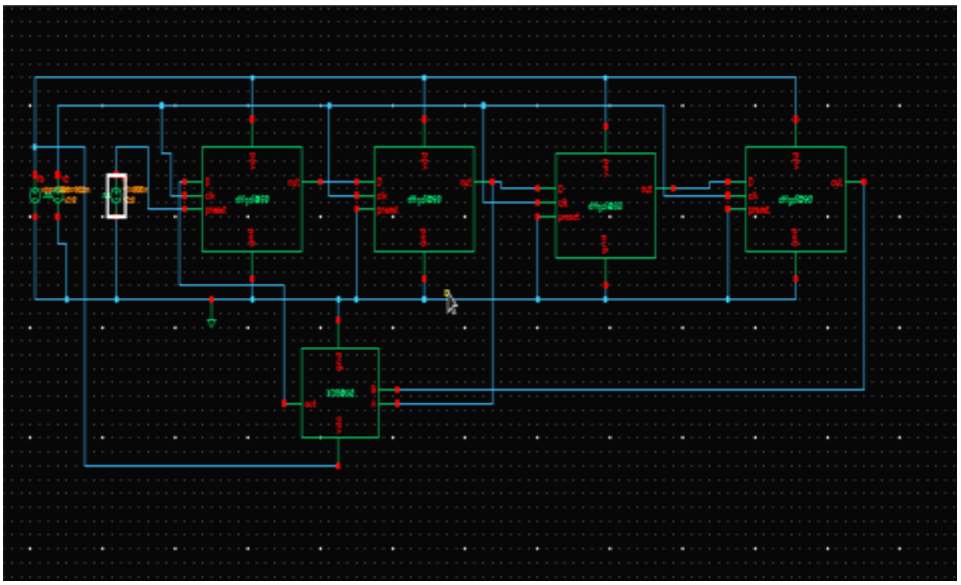

Fig. 12: GDI based LFSR Schematic using Cadence Virtuoso

IV. SIMULATION RESULTS

In this paper, average power and delay parameters are calculated for the 4-bit Linear Feedback Shift Register using Cadence Virtuoso with 90nm technology, simulation waveforms are obtained using digital schematic software and area layout can be viewed in the Micro Wind software.

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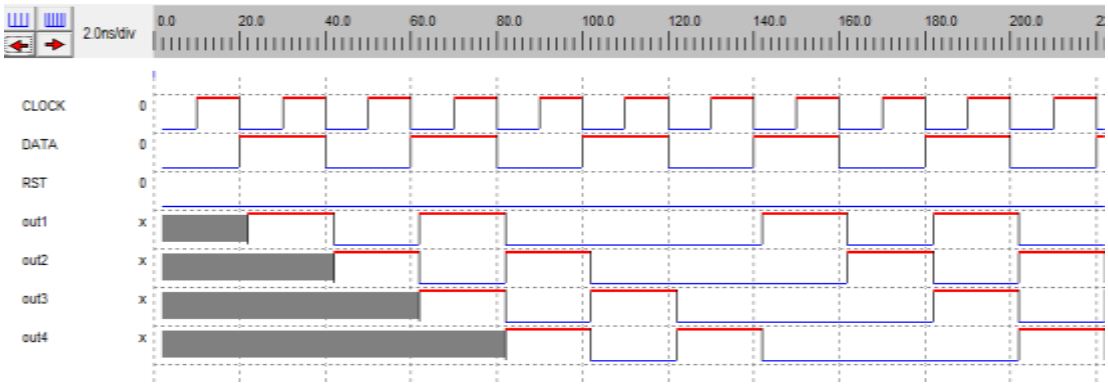

Fig. 13: Conventional 4-Bit LFSR Simulation Waveform

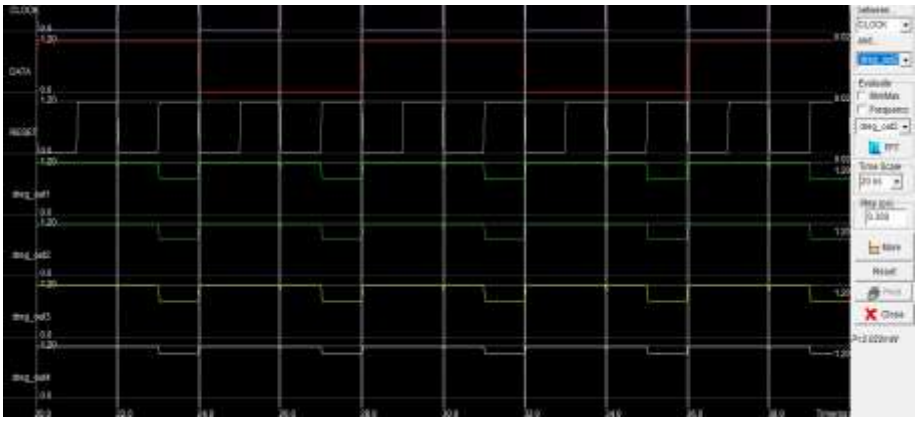

Fig. 14: Power Calculation of Conventional 4-Bit LFSR using Micro Wind

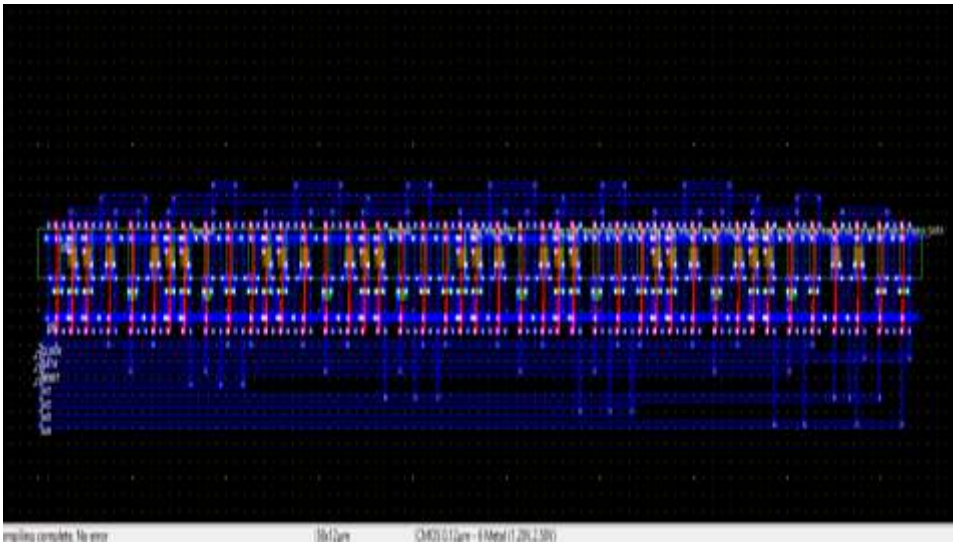

Fig. 15: Area Calculation of Conventional 4-Bit LFSR using Micro Wind

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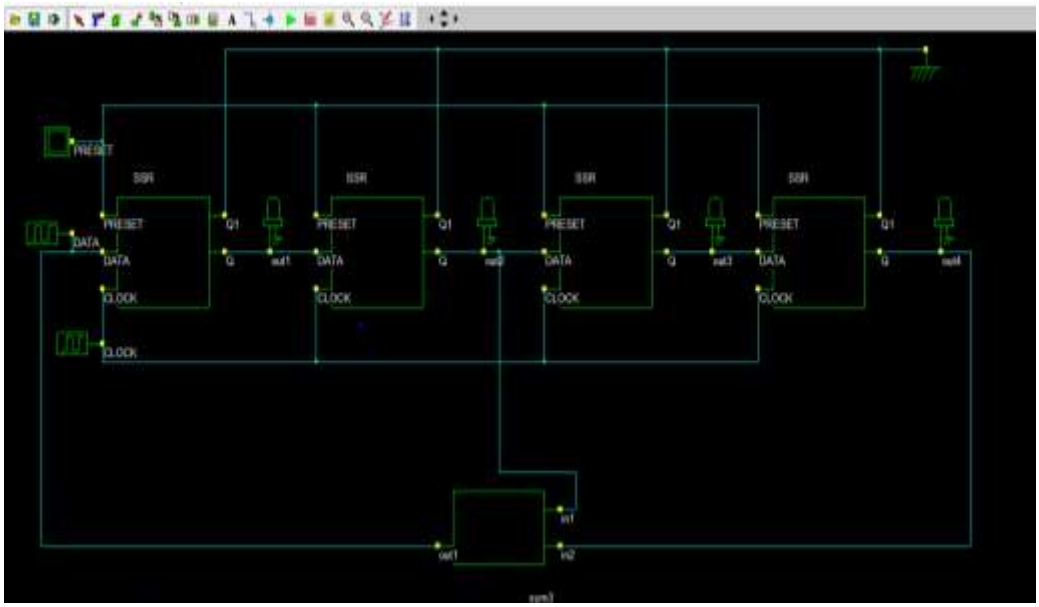

Fig. 16: GDI Based 4-Bit LFSR using Digital Schematic

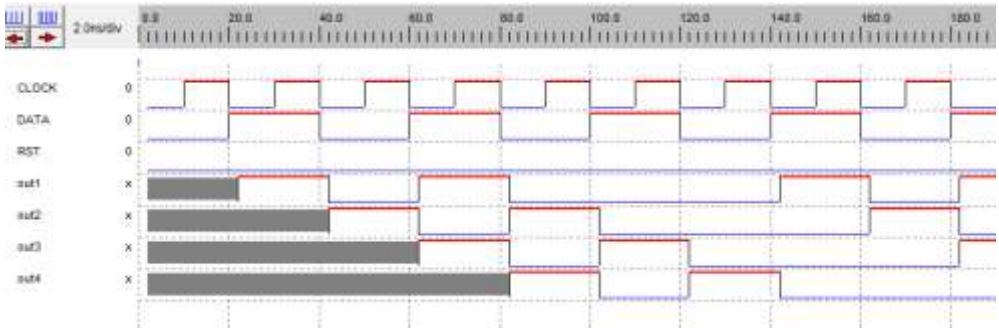

Fig. 17: Simulation Waveform of GDI based 4-Bit LFSR

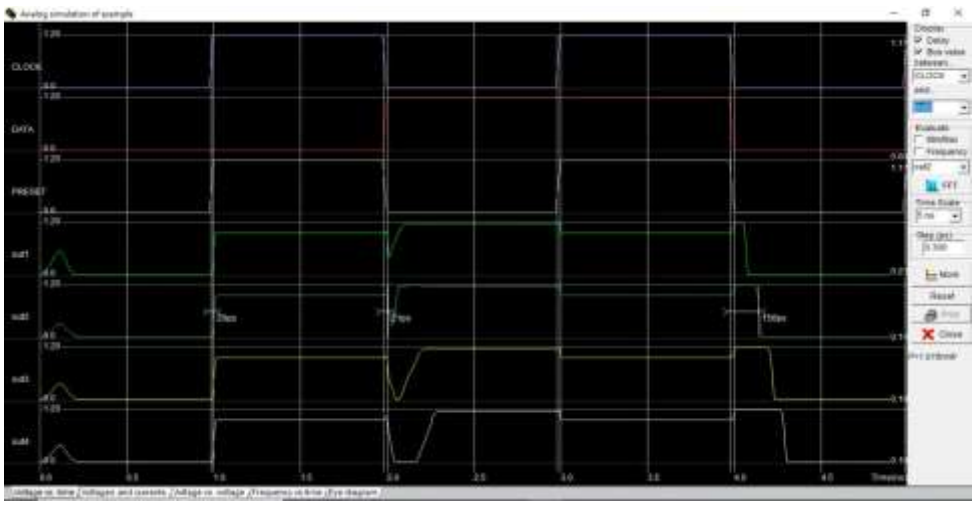

Fig. 18: GDI based LFSR Power Report using Micro Wind

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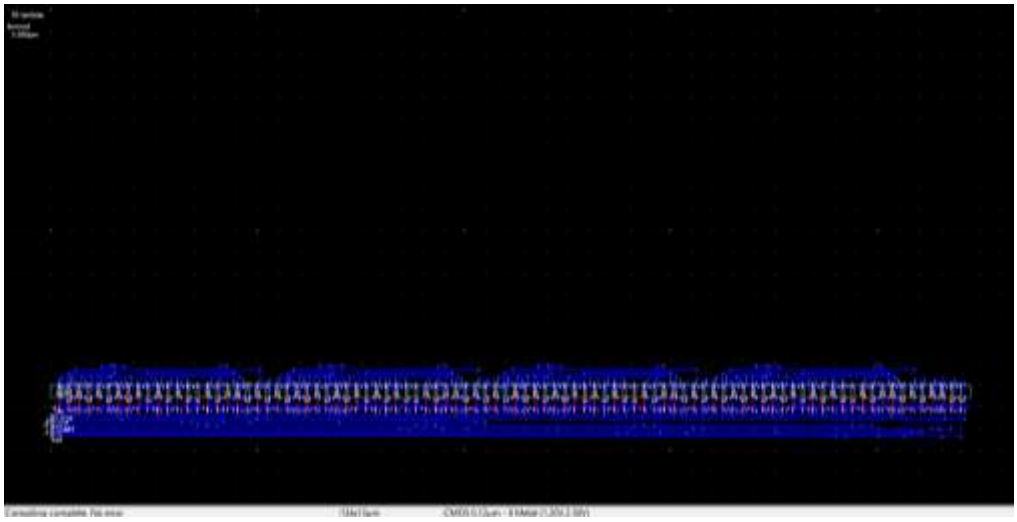

Fig. 19: GDI Based LFSR Area Report using Micro Wind

4.1. Proposed Hybrid 4-Bit LFSR using Digital Schematic

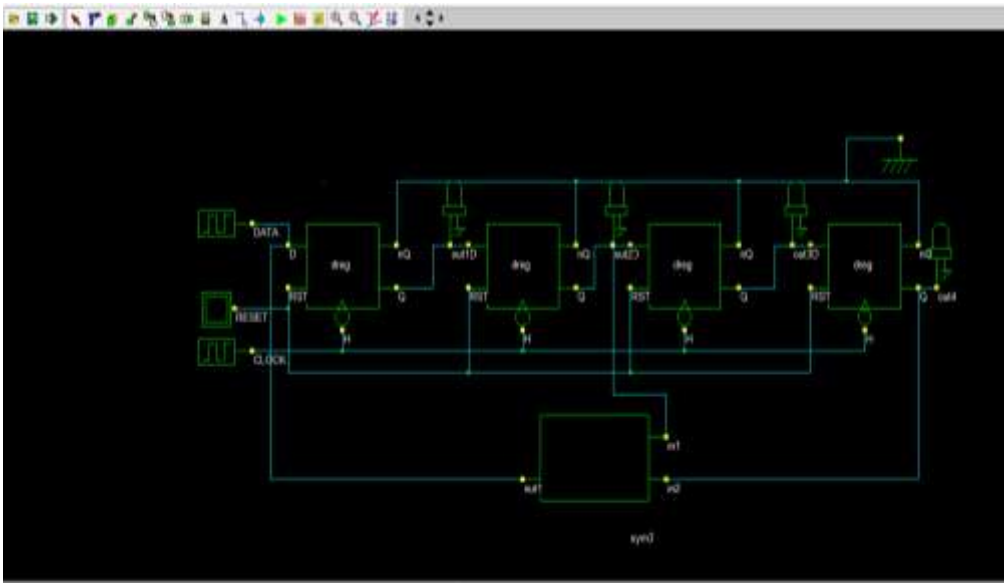

Fig. 20: Proposed Hybrid 4-Bit LFSR using Digital Schematic

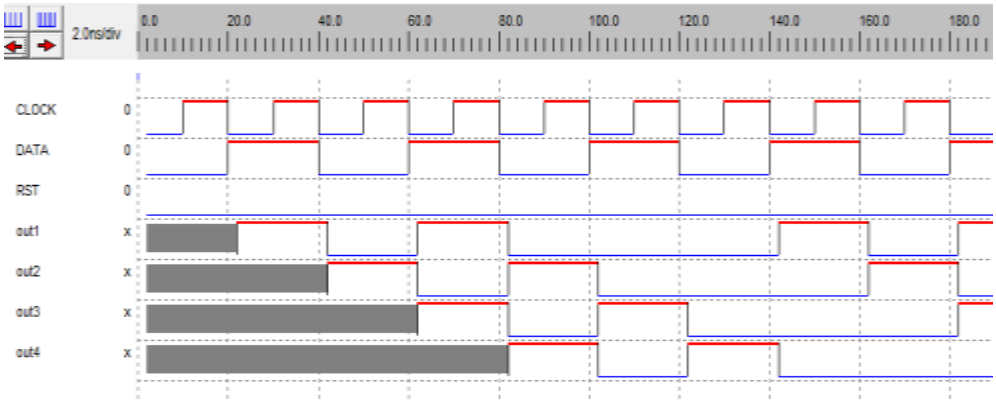

Fig. 21: Simulation Waveform of Proposed Hybrid 4-bit LFSR

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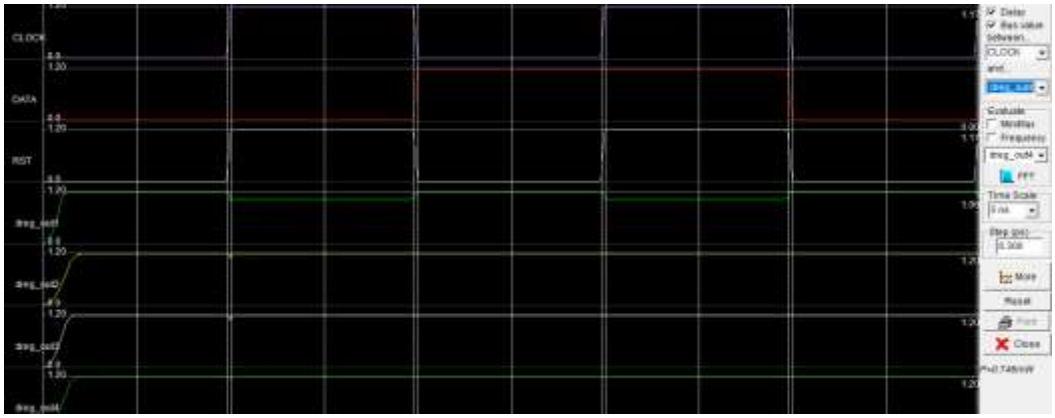

Fig. 22: Power Report of Proposed Hybrid LFSR using Micro Wind

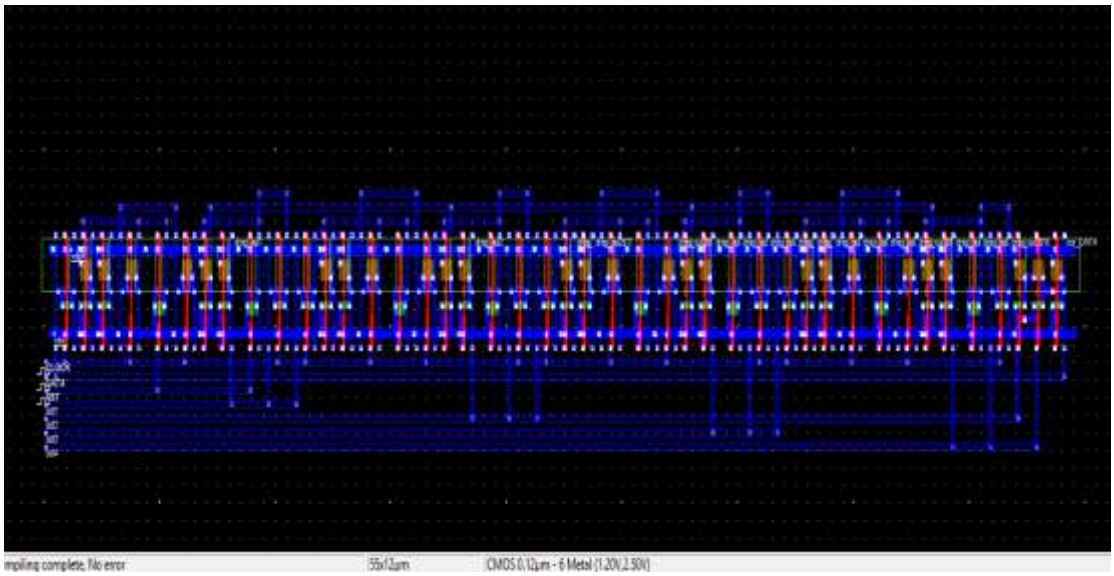

Fig. 23: Area Report of Proposed Hybrid 4-Bit LFSR using Micro Wind

4.2. Testing of Half Adder using 4-Bit LFSR

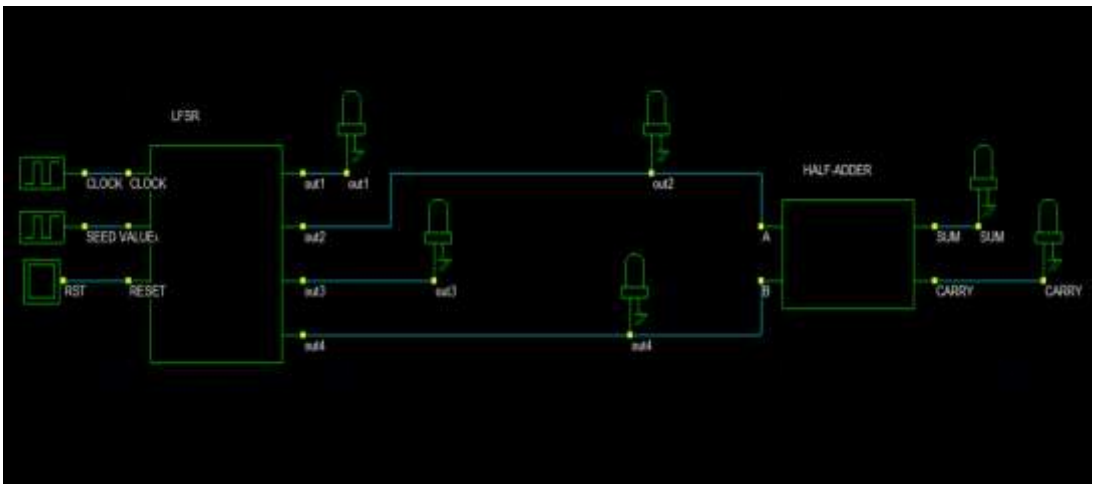

Fig. 24: Testing of Half adder using Proposed Hybrid 4-Bit LFSR

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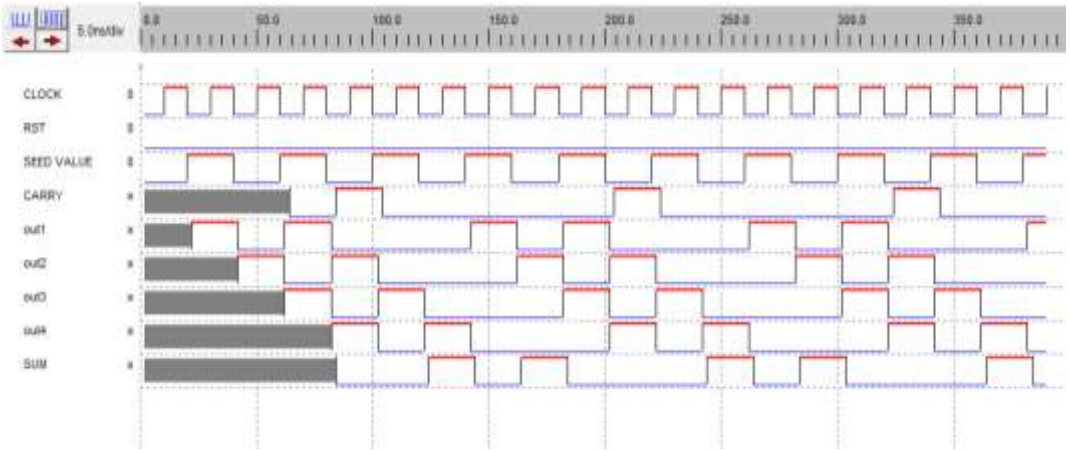

Fig. 25: Simulation Waveform of Half adder

4.3. Proposed Hybrid 4-Bit LFSR using Cadence 90nm Technology

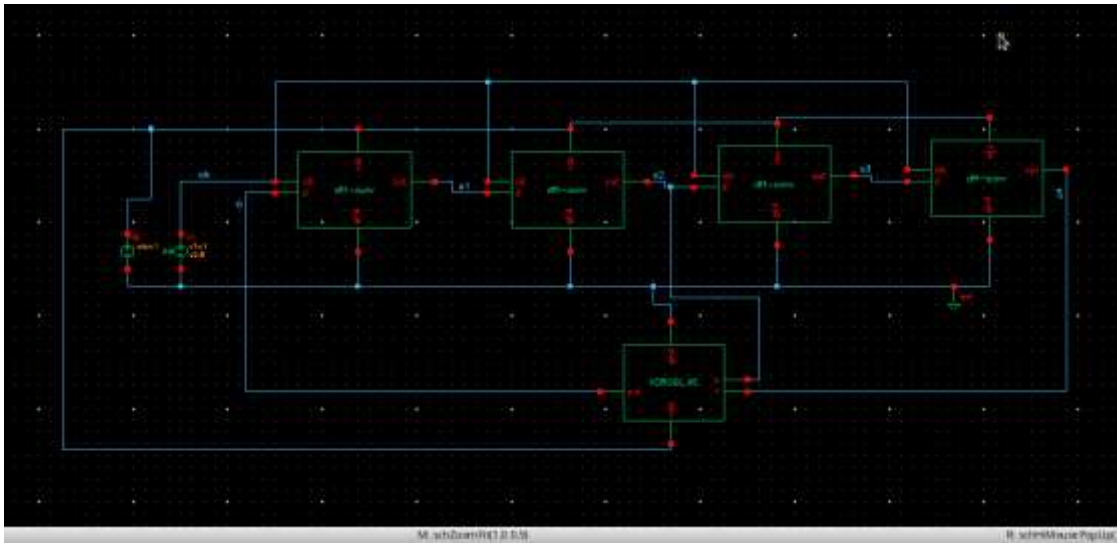

Fig. 26: Schematic Diagram of Proposed Hybrid 4-Bit LFSR using Cadence

Table. 2: Performance Analysis of different 4-Bit LFSR

PARAMETER	COMS	GDI	HYBRID
AVERAGE POWER	46.02 E-6	40.77 E-6	33.9 E-6
DELAY	3.35 E-3	1.498E-3	1.36 E-3

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Table. 3: Performance Analysis of different 4-bit LFSR

PARAMETER	AREA (µm)	POWER (mW)
CMOS	**58*12**	**2.022**
GDI	**134*13**	**1.018**
HYBRID	**55*12**	**0.746**

Table 2 shows the performance of average power and delay of 4-bit LFSR using Cadence. Table 3 shows the performance of area and power of 4-bit LFSR using Micro wind.

V. CONCLUSION & FUTURE SCOPE

In this paper, proposed hybrid 4-bit LFSR circuit designed and simulated using different Electronic Design Automation (EDA) tools. Further, the performance analysis done for all designs and results were shown in table 2 and table 3. Table 2 shows average power and delay values using Cadence tool, table 3 shows area and power values using Digital Schematic and Micro Wind tools. In this paper we proposed hybrid 4-bit LFSR to increase the competence, speed and to overcome the disadvantages of conventional and GDI based LFSR. From the simulation results, it is clearly observed that 62.12% power reduced compared to conventional LFSR, 26.71% power reduced compared to GDI, 59.40% delay reduced compared to conventional and 66.75 % delay reduced compared to GDI.

LFSR is used to generate random sequences which are very handy during testing of ASIC chips. In future, the proposed model may be suitable for Low Power VLSI design applications.

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